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PATENT APPLICATION

ADJUSTABLE THRESHOLD ISOLATION TRANSISTOR

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CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is a divisional of United States patent application number 09/016,157 filed January 30, 1998, which claims the benefit of United State provisional application number 60/044,243, filed April 23, 1997, both of which are incorporated by reference.

BACKGROUND

[0002] This invention relates, in general, to integrated circuit technology, and more particularly to isolation region transistors with variable threshold voltages.

[0003] Integrated circuits in general are plagued with certain parasitic characteristics. These characteristics often cause unintended results in the integrated circuit. In particular, parasitic transistors may occur on an integrated circuit where a conductive region carries a voltage over an isolation region that lies between two diffusion regions. As will be recognized, this structure forms a transistor. If the voltage on the conductive region is high enough, the transistor turns on and electricity conducts through a channel under the isolation region between the two diffusion regions.

[0004] In the past, such parasitic transistors were undesirable. To remove them, semiconductor designers implanted the areas under the isolation region with channel stop implants. The channel stop implants raised the threshold voltage above the voltage level on the conductive regions. However, it is desirable to find a beneficial use from such parasitic transistors.

[0005] Fig. 1 shows a cross-section of an integrated circuit 100 with a parasitic transistor. Two transistor devices 110 are separated by a field oxide 120. Field oxide 120 electrically isolates devices 110 from each other. Devices 110 are shown as transistors with source and drain regions and a polysilicon gate. However, these devices may be any active device, such as diodes, transistors, and the like. Devices 110 may reside in a doped well 125 used to electrically bias the environment of devices 110, or may be formed in an undoped substrate. Fig. 1 shows n-type devices residing in a p-type well, however the opposite configuration is also used to form p-type devices.

[0006] Conductive region 130 lies on top of field oxide 120. Conductive region 130 may be polysilicon, metal, or other conductive material. For example, conductive region 130 may be a polysilicon trace for carrying interconnection signals between various devices on integrated circuit 100. Consequently, at times, conductive region 130 may carry a voltage bias.

[0007] It will be recognized by one of skill in the art, that this structure forms a parasitic transistor. Conductive region 130 acts as a gate, the two diffusion regions of devices 110 as the source and drain, and field oxide 120 as an insulating layer under the gate. When a voltage of sufficient magnitude to overcome a threshold voltage is applied to conductive region 130, conduction may occur in a channel region between the two diffusion regions.

[0008] To compensate for this effect, it has been known to add a channel stop implant 140 beneath field oxide 120. Channel stop implant 140 is typically a doped material which raises the voltage threshold Vt of the parasitic transistor. Channel stop implant 140 is typically sufficient to raise Vt higher than any of the voltages used on the integrated circuit. Channel stop implant 140 is also known as a "field implant." Typically, with no channel stop implant 140, Vt of the parasitic transistor is approximately 8 volts to 10 volts. With channel stop implant 140, Vt is approximately 18 volts to 20 volts. In some embodiments, with no well 125 and no channel stop implant, Vt may be even lower, perhaps 2-3 volts.

[0009] One area in which presently available integrated circuits are limited is in their ability to handle voltages higher than the supply voltage (i.e., VDD.) Some integrated circuits, including programmable logic devices, EPROM memories, EEPROM memories, voltage pumps, etc. use higher voltages. For example, programmable logic device use Vpp, in a range from 6 volts to 16 volts, for programming logic functions. Currently available integrated circuits are limited in their ability to control devices using these higher voltages. Other high voltage problems, such as electrostatic discharge circuitry is also limited by currently available technology.

[0010] Consequently, new integrated circuit technology and methods for fabricating the integrated circuits are needed. In particular, a beneficial use for parasitic transistors is desirable.

SUMMARY

[0011] The present invention provides an integrated circuit device that uses parasitic transistors beneficially as isolation region transistors. The isolation region transistors can withstand high voltages without breaking down. The present invention also provides a method for fabricating

integrated circuits with isolation region transistors using existing integrated circuit fabrication processes.

[0012] The isolation region transistors are formed between the diffusion regions active devices. That is, the diffusion regions are the source and drain of the isolation region transistor, and a conductive region above an isolation region separating the diffusion regions is the gate. A channel stop implant is selectively implanted beneath the isolation region. This effectively provides a lower threshold voltage for the regions with no channel stop implant, compared with the threshold voltage for the regions with a channel stop implant. Thus, when the conductor carries sufficient voltage to exceed the threshold voltage in the regions with no channel stop implant, the isolation region transistor conducts, while the regions with the channel stop implant do not.

[0013] In a further embodiment of the present invention, a variable threshold isolation region transistor is provided. That is, the threshold voltage of an isolation region transistor may be varied using conventional integrated circuit fabrication methods. Briefly, the channel stop implant is formed in selected regions, but its length is varied, depending on the desired threshold voltage. Within a range, varying the length of the channel stop implant predictably varies the voltage threshold. The threshold voltage can be further varied by selectively placing the isolation region transistor in a doped well region.

[0014] The isolation region transistors provide, for example, a transistor device that can withstand higher voltages, such as the programming voltage Vpp, of an programmable integrated circuit. Especially advantageous is that the isolation region transistors can be fabricated with currently available and widely used fabrication processes. Further, many differing requirements may be addressed by the present invention, since the threshold voltage of the isolation region transistors may be varied from 2 volts to greater than 20 volts, again with no change to the fabrication process. This gives designers great flexibility, especially in high voltage designs.

[0015] A further understanding of the nature and advantages of the inventions herein may be realized by reference to the remaining portions of the specification and the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Fig. 1 shows a cross-section depicting a parasitic transistor in an integrated circuit;

[0017] Fig. 2 shows a digital system using the integrated circuit of the present invention;

[0018] Fig. 3A shows a cross-section of an isolation region transistor of the present invention with the channel stop implant removed;

[0019] Fig. 3B shows a cross-section of an isolation region transistor with the channel stop implant removed and no well;

[0020] Fig. 3C shows a circuit diagram for the integrated circuits of Figs. 3A and 3B;

[0021] Fig. 4 shows a planar view of two transistors with a conducting path controlled by an isolation region transistor of the present invention.

[0022] Fig. 5 is a graph plotting the voltage threshold against the length of the channel stop implant;

[0023] Fig. 6 is a flow diagram of a process for making an isolation region transistor according to the present invention; and

[0024] Figs. 7A-7J show cross sections of the integrated circuit during steps of the process of Fig. 6.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0025] Fig. 2 illustrates a typical environment in which an integrated circuit having been designed according to the principles of the present invention may be embodied. A digital system has a processing unit 180 that is coupled with a memory 185 and an input/output device 190. A personal computer is an example of such a digital system. However, a wide variety of electronic and consumer products will find beneficial use from the present invention. The present invention will find application in telecommunications, switches, networks, and many other areas of technology.

[0026] The digital system of Fig. 2 contains one or more integrated circuits 195 as described in the present invention. Integrated circuit 195 may be a programmable logic device, EPROM memory, EEPROM memory, Flash memory, microprocessor, controller, or a myriad of other integrated circuits. In Fig. 2, integrated circuit 195 is shown as a part of processing unit 180. However, memory 185 or input/output device 190 may also contain integrated circuit 195.

[0027] The digital system shown may be embodied on a single board, on multiple boards, or even within multiple enclosures. Furthermore, the digital system may comprise any multiple or combination of the devices shown. For example, the digital system may have multiple processing units 180, or have no processing unit 180 at all. One of the advantages of an

integrated circuit is its logical flexibility. Consequently, one with skill in the art can readily envision many applications for utilizing such a device within a variety of digital systems.

[0028] Fig. 3A shows a cross-section of a portion of integrated circuit 195. Integrated circuit 195 has two devices 110a and 110b (referred to collectively as devices 110) separated by field oxide 120. In Fig. 3A, devices 110 are transistor devices, but in other embodiments could be diodes, memory transistors, EPROM, EEPROM, or Flash memory cells, etc. Devices 110a and 110b may or may not be similar types of devices. Devices 110 are characterized by the existence of a diffusion region.

[0029] Devices 110 may reside in well 125 as shown in Fig. 3A, or may reside directly in the substrate of the integrated circuit as shown in Fig. 3B. Typically, well 125 is doped with a material of opposite polarity from a polarity of diffusion regions 314 of devices 110. Well 125 raises the magnitude of a voltage threshold Vt of devices residing in the well. In the specific embodiment shown, devices 110 are transistors with a gate 312 and n-type diffusion regions 314, and residing in a p-type well 125. However, it will be recognized that devices 110 may be n-type devices as in the specific embodiment, or p-type devices.

[0030] A conductor 130 is above field oxide 120. Conductor 130 may be polysilicon, metal, or other conductive material. It may be a conductive trace for carrying interconnection signals, power signals, I/O signals, and the like.

[0031] In contrast to integrated circuit 100 in Fig. 1, integrated circuit 195 in Fig. 3 has channel stop implant 140 (not shown in Fig. 3A) under only portions of field oxide 120. Channel stop implant 140 is formed by an implantation of ions of the polarity opposite that of diffusion regions 314. For example, for devices with n-type diffusion regions 314, boron may be implanted to form channel stop implant 140. Channel stop implant 140 is selectively not formed, or formed with a shorter length under other portions of field oxide 120. For example, the cross-section of Fig. 3A shows a portion with no channel stop implant.

[0032] Selective implantation of channel stop implant 140 for certain portions of integrated circuit 195 offers advantages over the prior art. Areas with no or less channel stop implant 140 form paths connecting devices 110. When sufficient voltage is applied to conductor 130, a conductive path 310 forms between devices 110 along the paths. In effect, this creates an isolation region transistor 320 with conductor 130 acting as a gate, and diffusion regions 314 of devices 110 acting as the source and drain. Conductive path 310 is the channel region and is

activated at a lower threshold voltage than those areas that have a traditional channel stop implant 140. As will be discussed further, the magnitude of the voltage threshold may be adjusted by varying the size of channel stop implant 140 and by the removal of well 125.

[0033] In operation, when the voltage on conductor 130 is below Vt of isolation region transistor 320, there is no conductive path between devices 110. Therefore, device 110a is decoupled from device 110b. When the voltage that is above Vt for isolation region transistor 320, but below Vt for the areas with channel stop implant 140, then conduction occurs along conductive path 310.

[0034] Isolation region transistor 320 may be controlled by higher voltages than typical MOS enhancement transistors. In the past, voltages of less than the supply voltage VDD were used on the transistor gates. Higher voltages would break down the transistors. However, the programming voltage Vpp of a programmable logic device, EEPROM, EPROM, or other nonvolatile storage device is typically higher than VDD. For example, Vpp may be in a range between 7 to 16 volts. Vpp may be generated internally or externally from the integrated circuit.

[0035] Using isolation region transistor 320 of the present invention, Vpp may be applied to conductor 130 over a field oxide 120 region with no channel stop implant 140 or shorter channel stop implants 140. This activates conductive path 310. As discussed above, this behavior is that of a transistor in the isolation region and is controlled by Vpp.

[0036] Isolation region transistor 320 with a high voltage threshold may be used in a variety of applications. For example, ESD structures, high-voltage switches, pumps, and voltage down-converters. Isolation region transistor 320 may be a p-type or n-type transistor. Use of n-type transistor is more common because high voltages are generally positive values. However, nothing in this specification is meant to limit the use to n-type isolation region transistors. The principles of the present invention may also be used for p-type isolation transistors. In this specification, references to decreasing or increasing voltages refer to the magnitude of the voltage.

[0037] Fig. 3B, shows isolation region transistor 320 formed in the substrate with no well 125. The elimination of well 125 decreases the threshold voltage of the isolation region transistor. Some applications may find use for the lower threshold voltage thereby provided. For example, such a device may be used for an over voltage protection circuit with almost no drop in voltage across the transistor due to Vt. By selectively adding well 125, varying the size of channel stop

implant 140, or completely removing channel stop implant 140, the voltage threshold can be adjusted over a wide range of voltages. Typically, this range may be from approximately two volts to greater than 20 volts.

[0038] Fig. 3C shows a circuit diagram for the portion of integrated circuit 195 shown in Figs. 3A and 3B. This diagram is reflective of the design shown in the above figures, but other configurations may also be envisioned in accordance with the present invention. In Fig. 3C, transistor devices 110 are separated by isolation region transistor 320. When a voltage of sufficient magnitude is applied to conductor 130, isolation region transistor 320 allows current to flow between its source and drain.

[0039] Fig. 4 shows a planar view (or layout) of a first transistor 410 and a second transistor 420 separated by an isolation region transistor 320 of the present invention. Field oxide 120 electrically isolates the two transistors 410 and 420 from each other and from an output pad 440. An isolation conductive path 310 connects transistors 410 and 420 together and to output pad 440. Isolation conductive path 310 is formed by a mask which allows channel stop implant 140 to be placed everywhere under field oxide 120 except in isolation conductive path 310.

[0040] Conductor 130 resides over field oxide 120 and acts as a transistor gate for isolation region transistor 320. When conductor 130 has a sufficient voltage, conductive path 310 allows electrical current to flow along isolation conductive path 310 from the two transistors 410 and 420 to output pad 440.

[0041] The first transistor 410 includes a first source/drain region 412 and a second source/drain region 414. A first isolation region under a first gate 418 isolates the first source/drain region 412 from the second source/drain region 414. The second transistor 420 includes a third source/drain region 422 and a fourth source/drain region 424. A second isolation region under a second gate 428 isolates the third source/drain region 422 from the fourth source/drain region 424. A third transistor, the isolation region transistor 320, includes a first drain (the second source/drain region 414), a second drain (the third source/drain region 422), and a source, which is a fifth source/drain region or output pad 440. A third isolation region under field oxide region 120 and third gate or conductor 130 isolates the second source/drain region 414 from the third source/drain region 422. The third isolation region also isolates the second source/drain region 414 and the third source/drain region 422 from the fifth source/drain region or output pad 440.

[0042] A possible use for this structure is, for example, in ESD discharge structures. When a high voltage ESD event occurs, the voltage rises on conductor 130 allowing electric charge to discharge from the transistors 410 and 420 to output pad 440. Output pad 440 may be connected to a strong ground. Isolation region transistors 320 may also be used, for example, as a charge pump when high voltages need to be maintained across oxides or junctions. High voltages are possible in this case, because the breakdown voltages of the field oxide are very high, for example 60 volts. Alternatively, as discussed above, the structure shown in Fig. 4 may be used to allow a high-voltages, such as the programming voltage Vpp, to control isolation region transistor 320.

[0043] Fig. 5 is a graph showing the voltage threshold for an isolation region transistor 320 plotted against the length of channel stop implant 140. This graph illustrates another aspect of the present invention. As can be seen, when the length of channel stop implant 140 is large (in comparison to the distance between adjacent devices), the voltage threshold is fairly constant. However, as the length of channel stop implant 140 decreases, the voltage threshold also decreases with a fairly linear slope. When the length of channel stop implant 140 is too small, the transistor begins to act as if there were no channel stop implant 140, and Vt is essentially identical to the intrinsic threshold voltage limits for the technology.

[0044] As can be seen in the graph, within a range 510, a change to the length of channel stop implant 140 causes a corresponding change to the voltage threshold of isolation region transistor 320. Accordingly, an integrated circuit designer may choose a specific threshold voltage, and adjust the length of channel stop implant 140 to give the desired threshold voltage.

[0045] Using this principle, an adjustable threshold device can be formed by changing the length of channel stop implant 140 according to the threshold voltage desired. No additional mask is required for forming these adjustable threshold devices so the impact to the design process and costs is minimal.

[0046] Fig. 6 shows a simplified flow diagram of a process for creating isolation region transistors 320 according to the present invention. Figs. 7A-7J show a simplified cross-section of the integrated circuit at each step in the process. It will be recognized that this is just an example of a method of making isolation region transistors 320. Techniques now known or later developed may be substituted or added to this method which are in keeping with the spirit and

scope of the present invention. This diagram is a brief description of the process, that will enable one of skill in the art to practice the invention.

[0047] The results of step 600 is shown in Fig. 7A. In step 600, the process grows a pad oxide layer 710 on the substrate. Pad oxide layer 710 is useful in a later step in which a field oxide is grown. Pad oxide layer 710 helps to prevent a silicon nitride layer from cracking during the growing of the field oxide.

[0048] Referring to Fig. 7B, in step 605, the process deposits a layer of silicon nitride 714 (Si3N4)on pad oxide 710. Silicon nitride 714 forms a barrier to be used in masking off the active areas of the integrated circuit. In step 610, an isolation mask covers silicon nitride 714 leaving exposed the areas in which a field oxide is desired. A solvent etches away the silicon nitride in the exposed areas. The results are depicted in Fig. 7C. In one embodiment of the present invention, a width 718 of the exposed area determines the voltage threshold for an isolation region transistor. By narrowing width 718, the length of the channel stop implant is shortened, lowering the voltage threshold as described above with respect to Fig. 5.

[0049] In step 630, spacer oxide is deposited. Openings are etched in the spacer oxide in those places in which a channel stop implant is desired. After etching, spacers 720 remain as shown in Fig. 7D. Spacers 720 shorten the length of the exposed area. The narrower exposed area define the area for deposition of channel stop implant 140. By narrowing the length of the exposed area, a gap will exist between the diffusion regions 314 and channel stop implant 140. Spacers 720 are grown by placing a layer of low temperature oxide LTO and anisotropically etching the LTO.

[0050] Referring to Fig. 7E, in step 640, channel stop implants 140 are formed by exposing the die to a dopant in those areas in which a channel stop implant is desirable. These areas are defined by a channel stop mask, as is known in the art. The dopant may be, for example, boron with a concentration of 1-2 x 1012 cm-2. Silicon nitride 714 and spacers 720 mask off the areas that are not to be implanted with channel stop implant 140.

[0051] As an alternative to narrowing the width of the field oxide region as discussed in step 610 for adjusting the threshold voltage, in a second embodiment, width 718 of the field oxide remains the same. In the second embodiment however, the length of channel stop implant 140 may be adjusted by changing the channel stop mask. By shortening the length of the mask openings, a smaller region is exposed during the implantation of channel stop 140 implants,

thereby adjusting the length of channel stop implants 140. As previously discussed, within a range, shorter channel stop implants cause the threshold voltage to be lower.

[0052] In step 650, spacers 720 are etched (wet) isotropically. This step removes spacers 720 so that the area for the isolation region is exposed as shown in Fig. 7F. Then, in step 660 and shown in Fig. 7G, the field oxide 120 is grown in the isolation region.

[0053] In step 670, silicon nitride 714 is stripped away as shown in fig. 7H. In step 675, a layer of polysilicon is deposited and a mask used to etch away polysilicon that is not desirable. Transistor gates and other conductors are formed in this fashion. Fig. 7I shows conductor 130, which is the gate for isolation region transistor 320 as one of the polysilicon conductors that may be formed in this step. Finally, in step 680, the diffusion regions 314 are implanted for the active devices as shown in Fig. 7J.

[0054] Of course, other steps such as the deposition of the polysilicon and metal layers, and the like, will also be done to complete the processing. However, these are not necessary to the understanding of this invention and are left out for simplicity. These processes are well known in the art.

[0055] An advantage to this process is that the designer has control over the voltage threshold without a process change from existing methods. Adjustments can be made to the layout design without adding new process steps or masks. This gives designers added flexibility, without any cost in terms of fabrication processes.

[0056] An apparatus and method of creating isolation region transistors has been disclosed. Specific embodiment has been taught using examples and drawings. It will be understood that the specific embodiments are given by way of example only, and are not meant to describe additional limitations above those given in the claims. It will be recognized by one of skill in the art that changes may be made to the examples shown, without departing from the spirit and scope of the present invention. Such changes are anticipated by this invention.